## LIST OF CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

1. (Previously Presented) An apparatus comprising:

a conditioning circuit that receives a clock signal and outputs a first pulse signal and a second pulse signal;

a tapped delay circuit including a plurality of tapped delay cells, said tapped delay circuit receiving the first pulse signal as input;

a plurality of sampling modules concurrently receiving the second pulse as input, each sampling module receiving said second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells; and

an encoder for generating an output value based on a number of sampling modules that lock into said second pulse signal.

2. (Original) The apparatus of claim 1, wherein said output value represents the process, voltage, and temperature (PVT) conditions of a microchip.

3. (Currently Amended) The apparatus of claim 1, further comprising:

an input for the clock signal;

wherein said conditioning circuit includes a counter for counting the cycles of said clock signal, ~~wherein~~ and said encoder generates said output value during predefined intervals defined by said clock signal.

4. (Previously Presented) The apparatus of claim 1, further comprising:

a variation circuit for receiving said generated output value and comparing said generated output value to a previously stored maximum output value and a previously stored minimum output value,

wherein, if said generated output value is less than said previously stored minimum output value, said generated output value is stored as said minimum output value, and

wherein if said generated output value is greater than said maximum output value, said generated output value is stored as said maximum output value.

5. (Original) The apparatus of claim 4, wherein said minimum output value and said maximum output value stored in said variation circuit represents a range of process, voltage, and temperature (PVT) conditions for a microchip.

6. (Original) The apparatus of claim 1, wherein said plurality of tapped delay cells includes at least one DELC1V15 delay component.

7. (Previously Presented) The apparatus of claim 1, further comprising:

a plurality of synchronizing elements for synchronizing the output signals from said plurality of sampling modules according to said clock signal,

wherein the outputs of said plurality of synchronizing elements are input to said encoder.

8. (Previously Presented) A variable delay circuit comprising:

a variable delay component for delaying an input signal, said variable delay component having a delay time that is controlled according to a control signal;

a delay compensation circuit for measuring the process, voltage and temperature (PVT) conditions of a microchip and outputting a value representative of said measured PVT conditions, comprising:

a conditioning circuit that receives a clock signal and outputs a first pulse signal and a second pulse signal;

a first tapped delay circuit including a plurality of first tapped delay cells, said first tapped delay circuit receiving said first pulse signal as input;

a plurality of sampling modules concurrently receiving said second pulse as input, each sampling module receiving said second pulse signal as input while said first pulse signal propagates through said first tapped delay circuit; each sampling module being clocked by a first tapped output signal from one of said plurality of first tapped delay cells;

wherein said output value representative of said measure PVT conditions is used to generate said control signal for said variable delay component.

9. (Previously Presented) The variable delay circuit of claim 8, wherein said variable delay component is a second tapped delay circuit, which includes

a plurality of second tapped delay cells connected in series;

and a multiplexor for selecting and outputting a second tapped signal from one of said plurality of second tapped delay cells based on said control signal.

10. (Previously Presented) The variable delay circuit of claim 9, wherein said plurality of second tapped delay cells includes at least one DELC1V15 delay component.

11. (Previously Presented) The variable delay circuit of claim 8, wherein said delay compensation circuit further comprises:

an encoder for outputting said value representative of PVT conditions based on a number of sampling modules that lock into said second pulse signal.

12. (Currently Amended) The variable delay circuit of claim 11, wherein said delay compensation circuit further includes

an input for said clock signal;

wherein said conditioning circuit includes a counter for counting the cycles of said clock signal, ~~wherein~~ and said encoder generates said output value during predefined intervals defined by said clock signal.

13. (New) An apparatus comprising:

a variation circuit for receiving a generated output value and comparing said generated output value to a previously stored maximum output value and a previously stored minimum output value,

wherein, if said generated output value is less than said previously stored minimum output value, said generated output value is stored as said minimum output value, and

wherein if said generated output value is greater than said maximum output value, said generated output value is stored as said maximum output value.